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CENTRAL FAX CENTER**Attorney Docket No.: N1280-00670  
App. Serial No.: 10/781,107

SEP 26 2007

**Amendments to the Claims:**

The claims in this listing will replace all prior claims in the application.

1. (currently amended) A method for inspecting defects in a wafer, the method comprising:

acquiring at least one digitized image of at least one actual feature on the wafer taken directly from the portion of a wafer;

converting at least one design database file corresponding to the feature portion of the wafer into at least one inspection file;

setting one or more error detection thresholds; and

comparing the digitized image and the inspection file by an inspection tool for detecting defects with regard to the feature portion of the wafer based on the set error detection thresholds.

2. (original) The method of claim 1 wherein the design database file is processed with optical proximity correction features.

3. (original) The method of claim 1 wherein the converting further includes converting the design database file to an aerial image format.

4. (currently amended) The method of claim 3 ~~wherein~~ further comprising includes converting the database file from the aerial image format to an inspection file format.

5. (original) The method of claim 1 further comprising bias fitting the digitized image and/or the converted inspection file to render both files to be comparable by the inspection tool.

Attorney Docket No.: N1280-00670  
App. Serial No.: 10/781,107

6. (original) The method of claim 1 further comprising detecting a proximity trend with the portion of the wafer.

7. (original) The method of claim 1 wherein the defects include mask patterning induced defects.

8. (original) The method of claim 1 wherein the defects include wafer processing induced defects.

9. (original) The method of claim 1 wherein the defects include circuit layout induced defects.

10. (currently amended) A method for inspecting mask patterning process induced defects in a wafer, the method comprising:

acquiring at least one digitized image of at least one actual feature on the wafer taken directly from the wafer at least one mask pattern;

converting at least one mask database file for a mask corresponding to the feature mask pattern into at least one inspection file specific to an inspection tool through an aerial image based processing;

comparing the digitized image and the inspection file by the inspection tool; and  
detecting disallowed mask patterning process induced defects by examining differences.

11. (original) The method of claim 10 wherein the detecting further includes detecting defects induced by one or more processes using the mask.

**Attorney Docket No.: N1280-00670**  
**App. Serial No.: 10/781,107**

12. (original) The method of claim 10 wherein the detecting further includes detecting defects induced by a mask writer while making the mask.

13. (original) The method of claim 10 wherein the detecting further includes detecting defects induced by a mask blank substrate.

14. (original) The method of claim 10 wherein the detecting further includes detecting proximity trends of the mask pattern.

15. (currently amended) A method for inspecting wafer processing induced defects for making a semiconductor device, the method comprising:

acquiring at least one digitized image of at least one actual feature on the wafer taken directly from the wafer;

converting at least one design database file corresponding to the feature into at least one inspection file specific to an inspection tool through an aerial image based processing;

comparing the digitized image and the inspection file by the inspection tool; and

detecting disallowed wafer processing induced defects by examining differences between the inspection file and the digitized image corresponding to the feature.

16. (original) The method of claim 15 wherein the defects includes critical dimension errors.

Attorney Docket No.: N1280-00670  
App. Serial No.: 10/781,107

17. (original) The method of claim 15 further includes information about critical dimension distribution.

18. (original) The method of claim 15 further comprising bias fitting the digitized image and/or the inspection file.

19. (original) The method of claim 15 wherein the detecting further includes setting on or more error detection thresholds for avoiding false defects.

20. (currently amended) A method for inspecting circuit layout related defects for making a semiconductor device, the method comprising:

acquiring at least one digitized image of at least one actual circuit feature on the wafer taken directly from the wafer;

converting at least one circuit design database file corresponding to the feature based on one circuit layout design into at least one inspection file through an aerial image based processing;

comparing the digitized image and the inspection file by the inspection tool; and  
detecting disallowed circuit layout related defects by examining differences thereof.